REMARKS

Claims 1-2 and 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Van Brunt (U.S. Patent Number 4,357,703). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention of claims 1 and 2, a semiconductor integrated circuit includes a plurality of data input pins which receive data signals in a normal mode and at least one of the plurality of data input pins receives test signals in a test mode, such that the data input pins can receive both the data signals and the test signals.

Claims 1 and 2 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the data input pins receive data signals in the normal mode and at least one of the plurality of data input pins receives test signals in the test mode, such that the data input pins can receive both the data signals and the test signals. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention of claims 5 and 6, a method for receiving test data signals and outputting data in a test mode of a semiconductor integrated circuit includes receiving data signals at a plurality of data input pins during a normal mode and receiving the test data signals at the plurality of data input pins during the test mode, such that the data input pins can receive both the data signals and the test signals.

Claims 5 and 6 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the method includes receiving the data signals at the plurality of data input pins during the normal mode and receiving the test data signals at the plurality of data input pins during the test mode, such that the data input pins can receive both the data signals and the test signals. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Van Brunt discloses an LSI logic module. Main function inputs to the LSI chip are provided on a plurality of input lines 12, and a test data input pin 21 receives serialized test data. Normal data input from the main function input terminals 12 is prohibited during a test mode, and serialized test data is received through test data input pin 21 during the test mode.

Van Brunt fails to teach or suggest a semiconductor integrated circuit that includes a plurality of data input pins which receive data signals in a normal mode and at least one of the plurality of data input pins receiving test signals in a test mode, such that the data input pins can receive both the data signals and the test signals, as claimed in claims 1 and 2. Van Brunt also fails to teach or suggest a method that includes receiving data signals at a plurality of data input pins during a normal mode and receiving test data signals at the plurality of data input pins during a test mode, such that the data input pins can receive both the data signals and the test signals, as claimed in claims 5 and 6. Instead, in Van Brunt, the main function inputs are received at input lines 12, and the serialized test data is received at the separate test data input pin 21.

Van Brunt fails to teach or suggest certain elements of the invention set forth in claims 1, 2, 5 and 6. Specifically, Van Brunt fails to teach or suggest a semiconductor integrated circuit that includes a plurality of data input pins which receive data signals in a normal mode and at least one of the plurality of data input pins receiving test signals in a test mode, such that the data input pins can receive both the data signals and the test signals, as claimed in claims 1 and 2. Van Brunt further fails to teach or suggest a method that includes receiving data signals at a plurality of data input pins during a normal mode and receiving test data signals at the plurality of data input pins during a test mode, such that the data input pins can receive both the data signals and the test signals, as claimed in claims 5 and 6. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 1, 2, 5 and 6 under U.S.C. 102(b) as being anticipated by Van Brunt is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is

respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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